3/Preandta P. Walker 1-8-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

TC 2800 MAIL ROOM

In re Application of:

Michael B. Ball

Serial No.: 09/943,880

Filed: August 30, 2001

For: METHOD OF FABRICATION OF STACKED SEMICONDUCTOR DEVICES

Examiner: Unknown

Group Art Unit: 2814

Attorney Docket No.: 2769.6US (95-1118.5)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail (under 37 C.F.R. § 1.8(a)) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231.

November 13, 2001
Date of Deposit

Bonnie L. Huntsman
Signature of registered practitioner or other person having reasonable basis to expect mailing to occur on date of deposit shown pursuant to 37 C.F.R. § 1.8(a)(1)(ii)

Bonnie L. Huntsman
Typed/printed name of person whose signature is contained above

PRELIMINARY AMENDMENT

Box Non-Fee Amendment
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-referenced patent application on the merits, entry of the amendments as set forth herein is respectfully solicited.

IN THE SPECIFICATION:

Please replace Paragraph **[0001]** with the following:

a1

[0001] This application is a continuation of application Serial No. 09/651,394, filed August 29, 2000, pending, which is a continuation of U.S. Patent Application Serial No. 08/844,669 filed April 18, 1997, now U.S. Patent 6,165,815, issued December 26, 2000, which is a continuation of U.S. Patent Application Serial No. 08/650,429, filed May 20, 1996, abandoned.

IN THE CLAIMS:

Claims 1, 4-5, 10-12 and 18-19 have been amended herein. All of the pending claims 1 through 24 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Also attached is a marked-up version of the claims amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

---

q2

1. (Amended) A method of fabricating a multi-level stack of semiconductor substrate elements, each of said elements including integrated circuitry, comprising:

providing a first semiconductor substrate element having a first side including integrated circuitry thereon and having a back side;

providing at least one second semiconductor substrate element having a first side including a plurality of integrated circuitry thereon and having a backside;

stacking said first semiconductor element and said at least one second semiconductor substrate element in a superimposed relationship having the back side of the first semiconductor substrate element facing the back side of the at least one second semiconductor substrate element aligning vertically said first semiconductor substrate element and the at least one second semiconductor substrate element to vertically align integrated circuitry on said first semiconductor substrate element and at least one of the plurality of integrated circuits on said at least one second semiconductor substrate element and severing from said stack traversely at least one dice pair comprising a die from said first semiconductor substrate element and an aligned second die from said at least one second semiconductor substrate element; and

adhesively attaching said first semiconductor substrate element and said at least one second semiconductor substrate element.

---

2. The method of claim 1, wherein said adhesive comprises a dielectric adhesive.

3. The method of claim 1, further including:
disposing a heat sink element between said first semiconductor substrate element and said at least one second semiconductor substrate element.

a3

4. (Amended) The method of claim 1, wherein said first semiconductor substrate element and at least one second semiconductor substrate element, each element including locations defining discrete dice or wafer portions severable from a first semiconductor substrate wafer and at least one second substrate wafer.

5. (Amended) The method of claim 1, wherein said first semiconductor substrate element and said at least one second semiconductor substrate element each include a flat, and said vertical alignment is effected by aligning said flat of said first semiconductor substrate element and said flat of the at least one second semiconductor substrate element.

6. The method of claim 1, further comprising:
connecting a first die of said at least one dice pair to conductors of a substrate.

7. The method of claim 6, wherein said connection is selected from a group comprising reflowable metal elements, polymer elements having a conductive capability, and preformed lead-type elements.

8. The method of claim 6, further comprising:
connecting both dice of said at least one dice pair to conductors of said substrate.

9. The method of claim 1, further comprising:
connecting the second die of said at least one dice pair to conductors of said substrate through intermediate connection elements.

A4 Contd

10. (Amended) The method of claim 9, wherein said intermediate connection elements are selected from a group consisting of bond wires and traces of flex circuits.

11. (Amended) The method of claim 10, further comprising:

connecting said at least one dice pair to conductors of said substrate and encapsulating said at least one dice pair thereafter.

12. (Amended) A method of fabricating a multi-level stack of semiconductor wafer segments, each of said semiconductor wafer segments including integrated circuitry, comprising:

providing a first semiconductor substrate segment having a first side including integrated circuitry thereon and having a back side;

providing at least one second semiconductor substrate segment having a first side including a plurality of integrated circuits thereon and having a backside;

stacking said first semiconductor substrate segment and said at least one second semiconductor substrate segment in at least partially superimposed relationship to form a stack of semiconductor wafer segments;

separating said stack to form at least two semiconductor wafer segment stacks, each said semiconductor wafer segment stack comprising a first semiconductor wafer segment having a side including integrated circuitry and a back side and at least one second semiconductor wafer segment having a side including integrated circuitry and a back side,

stacking said at least two semiconductor wafer segment stacks in at least partially superimposed relationship;

locating bond pads on said first semiconductor wafer segment of at least one of said at least two semiconductor wafer segment stacks on a side adjacent said at least one second semiconductor wafer segment of said at least one semiconductor wafer segment stack at a periphery thereof;

forming a notch through said at least one second semiconductor wafer segment of said at least one semiconductor wafer segment stack, said notch extending between and substantially

Q4 end

perpendicular to a circuitry side and a back side of said at least one second semiconductor wafer segment to provide access to at least one said peripheral bond pad of said first semiconductor wafer segment of said at least one semiconductor wafer segment stack; and

adhesively attaching said first and said at least one second semiconductor wafer segments of said at least one semiconductor wafer segment stack.

13. The method of claim 12, further including:

stacking said semiconductor wafer segments of said at least one semiconductor wafer segment stack with the integrated circuitry side of said first semiconductor wafer segment proximate the back side of said at least one second semiconductor wafer segment; and

locating said bond pads on said integrated circuitry side of said first semiconductor wafer segment.

14. The method of claim 12, further including:

adhesively attaching said first and said at least one second semiconductor wafer segments of said at least one semiconductor wafer segment stack.

15. The method of claim 12, further including

disposing a heat sink element between said first and said at least one second semiconductor wafer segments.

16. The method of claim 12, further comprising:

connecting at least one of said first and said at least one second semiconductor wafer segment to conductors of a substrate.

17. The method of claim 16, wherein said connection comprises a connection element selected from a group comprising bond wires and traces of flex circuits.

a5

18. (Amended) A method of fabricating a multi-level stack of semiconductor wafers, each of said semiconductor wafers including integrated circuitry, comprising:

providing a first semiconductor wafer having a first side including integrated circuitry and having a back side;

providing at least one other semiconductor wafer having a first side including integrated circuitry and having a back side;

stacking said first semiconductor wafer and said at least one other semiconductor wafer in a superimposed relationship;

locating bond pads on said first semiconductor wafer of said stack on a side proximate said at least one other semiconductor wafer at a periphery thereof;

forming a notch through said at least one other semiconductor wafer, said notch substantially perpendicular to a circuitry side and the back side of said at least one other semiconductor wafer providing access to at least one said peripheral bond pads of said first semiconductor wafer of said stack; and

adhesively attaching said first semiconductor wafer and said at least one other semiconductor wafer.

19. (Amended) The method of claim 18, further including:

stacking said first semiconductor wafer and said at least one other semiconductor wafer with a third semiconductor wafer, having the integrated circuitry side of said first semiconductor wafer segment proximate said back side of said third semiconductor wafer.

20. The method of claim 18, wherein said adhesively attaching said first semiconductor wafer and said at least one other semiconductor wafer comprises:

adhesively attaching said first semiconductor wafer and said at least one other semiconductor wafer with a dielectric adhesive.

21. The method of claim 18, further including:

disposing a heat sink element between said first semiconductor wafer and said at least one other semiconductor wafer.

22. The method of claim 18, further comprising:

connecting at least one of said first semiconductor wafer and said at least one other semiconductor wafer to conductors of a substrate.

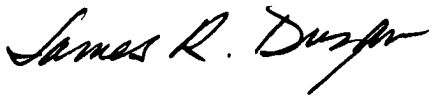
23. The method of claim 22, wherein a direct electrical connection is achieved with a connection element selected from a group comprising bond wires and traces of flex circuits.

24. The method of claim 18, wherein said first semiconductor wafer and said at least one other semiconductor wafer are stacked with the integrated circuit side of said first semiconductor wafer facing the back side of said at least one other semiconductor wafer, and wherein said bond pads are located on the integrated circuit side of said first semiconductor wafer.

REMARKS

No new matter has been added. The Applicant again requests entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,



James R. Duzan
Registration No. 28,393
Attorney for Applicant
TRASKBRITT
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: November 13, 2001
JRD/dn/blh

N:\2269\2769.6\PRELIM.AMD

Enclosures: Version of Specification with Markings to Show Changes Made
Version of Claims with Markings to Show Changes Made